

# PFE modular front-end cards

for Zynq UltraScale+ RFSoc evaluation kits by AMD Xilinx

PFE is a modular front-end solution for the evaluation kits of the 3rd generation Zynq UltraScale+ RFSoc devices by AMD Xilinx. The PFE boards are manufactured with high-quality, ultralow-loss PCB laminates for high-frequency analog signals.

The PFE solution consists of the base board pfe-base that mates to the RFSoc evaluation board, and of several module boards that mate to the pfe-base.

## General handling

Ensure the RFSoc EK is powered off before connecting pfe-base or changing any pfe modules. Permanent damage to this product and/or to the RFSoc EK can occur if this product is hot swapped.

Modules should be mechanically secured to the provided PFE support panel or similar enclosure front panel support with nuts on each SMA connector prior to use.

Use SMA torque wrench with max 0.5 N·m to fasten cables to the connectors. Excessive torque can damage the device.

## Detailed description

### pfe-base

#### Compatibility

The base board pfe-base is compatible with the RFSoc evaluation kits ZCU216 (EK-U1-ZCU216-V1-G) and ZCU208 (EK-U1-ZCU208-V1-G), and the RFSoc DFE evaluation kit ZCU670 (EK-U1-ZCU670-V2-G).

#### RFMC connectors

Pfe-base mates to the ZCU board via two RFMC 2.0 connectors J13 and J15. These are LPAM-50-01.0-L-08-2-K-TR by Samtec.

#### Module connectors

Pfe-base has eight board-to-board connectors J17–J24 for mating with the PFE modules. These connectors are optimized for high-frequency differential pairs such as the RF analog signals from the RFSoc. The RF signals available in each module depend on the type of ZCU board used, see tables below.

## ZCU216

<u>Pin number</u>	<u>J17, DAC228</u>	<u>J18, DAC229</u>	<u>J19, DAC230</u>	<u>J20, DAC231</u>
3, 5	VCC12_SW	VCC12_SW	VCC12_SW	VCC12_SW
4, 6	UTIL_5V0	UTIL_5V0	UTIL_5V0	UTIL_5V0
9, 11	UTIL_3V3	UTIL_3V3	UTIL_3V3	UTIL_3V3
10, 12	VCC1V8_BUS	VCC1V8_BUS	VCC1V8_BUS	VCC1V8_BUS
15, 16, 17, 18	GPIO	GPIO	GPIO	GPIO
30	DAC228_T0_CH0_N	DAC229_T1_CH0_N	DAC230_T2_CH0_N	DAC231_T3_CH0_N
32	DAC228_T0_CH0_P	DAC229_T1_CH0_P	DAC230_T2_CH0_P	DAC231_T3_CH0_P
35	DAC228_T0_CH1_P*	DAC229_T1_CH1_P*	DAC230_T2_CH1_P*	DAC231_T3_CH1_P*
37	DAC228_T0_CH1_N*	DAC229_T1_CH1_N*	DAC230_T2_CH1_N*	DAC231_T3_CH1_N*
42	DAC228_T0_CH2_N	DAC229_T1_CH2_N	DAC230_T2_CH2_N	DAC231_T3_CH2_N
44	DAC228_T0_CH2_P	DAC229_T1_CH2_P	DAC230_T2_CH2_P	DAC231_T3_CH2_P
47	DAC228_T0_CH3_P*	DAC229_T1_CH3_P*	DAC230_T2_CH3_P*	DAC231_T3_CH3_P*
49	DAC228_T0_CH3_N*	DAC229_T1_CH3_N*	DAC230_T2_CH3_N*	DAC231_T3_CH3_N*
others	GND	GND	GND	GND

<u>Pin number</u>	<u>J21, ADC224</u>	<u>J22, ADC225</u>	<u>J23, ADC226</u>	<u>J24, ADC227</u>
3, 5	VCC12_SW	VCC12_SW	VCC12_SW	VCC12_SW
4, 6	UTIL_5V0	UTIL_5V0	UTIL_5V0	UTIL_5V0
9, 11	UTIL_3V3	UTIL_3V3	UTIL_3V3	UTIL_3V3
10, 12	VCC1V8_BUS	VCC1V8_BUS	VCC1V8_BUS	VCC1V8_BUS
15, 16, 17, 18	GPIO	GPIO	GPIO	GPIO
30	ADC224_T0_CH0_N	ADC225_T1_CH0_N	ADC226_T2_CH0_N	ADC227_T3_CH0_N
32	ADC224_T0_CH0_P	ADC225_T1_CH0_P	ADC226_T2_CH0_P	ADC227_T3_CH0_P
35	ADC224_T0_CH1_P*	ADC225_T1_CH1_P*	ADC226_T2_CH1_P*	ADC227_T3_CH1_P*
37	ADC224_T0_CH1_N*	ADC225_T1_CH1_N*	ADC226_T2_CH1_N*	ADC227_T3_CH1_N*
42	ADC224_T0_CH2_N	ADC225_T1_CH2_N	ADC226_T2_CH2_N	ADC227_T3_CH2_N
44	ADC224_T0_CH2_P	ADC225_T1_CH2_P	ADC226_T2_CH2_P	ADC227_T3_CH2_P
47	ADC224_T0_CH3_P*	ADC225_T1_CH3_P*	ADC226_T2_CH3_P*	ADC227_T3_CH3_P*
49	ADC224_T0_CH3_N*	ADC225_T1_CH3_N*	ADC226_T2_CH3_N*	ADC227_T3_CH3_N*
23	VCM23_224	VCM23_225	VCM23_226	VCM23_227
24	VCM01_224	VCM01_225	VCM01_226	VCM01_227
others	GND	GND	GND	GND

## ZCU208

<u>Pin number</u>	<u>J17, DAC228</u>	<u>J18, DAC229</u>	<u>J19, DAC230</u>	<u>J20, DAC231</u>
3, 5	VCC12_SW	VCC12_SW	VCC12_SW	VCC12_SW
4, 6	UTIL_5V0	UTIL_5V0	UTIL_5V0	UTIL_5V0
9, 11	UTIL_3V3	UTIL_3V3	UTIL_3V3	UTIL_3V3
10, 12	VCC1V8_BUS	VCC1V8_BUS	VCC1V8_BUS	VCC1V8_BUS
15, 16, 17, 18	GPIO	GPIO	GPIO	GPIO
30	DAC228_T0_CH0_N	DAC229_T1_CH0_N	DAC230_T2_CH0_N	DAC231_T3_CH0_N
32	DAC228_T0_CH0_P	DAC229_T1_CH0_P	DAC230_T2_CH0_P	DAC231_T3_CH0_P
35	NC	NC	NC	NC
37	NC	NC	NC	NC
42	DAC228_T0_CH2_N	DAC229_T1_CH2_N	DAC230_T2_CH2_N	DAC231_T3_CH2_N
44	DAC228_T0_CH2_P	DAC229_T1_CH2_P	DAC230_T2_CH2_P	DAC231_T3_CH2_P
47	NC	NC	NC	NC
49	NC	NC	NC	NC
others	GND	GND	GND	GND

<u>Pin number</u>	<u>J21, ADC224</u>	<u>J22, ADC225</u>	<u>J23, ADC226</u>	<u>J24, ADC227</u>
3, 5	VCC12_SW	VCC12_SW	VCC12_SW	VCC12_SW
4, 6	UTIL_5V0	UTIL_5V0	UTIL_5V0	UTIL_5V0
9, 11	UTIL_3V3	UTIL_3V3	UTIL_3V3	UTIL_3V3
10, 12	VCC1V8_BUS	VCC1V8_BUS	VCC1V8_BUS	VCC1V8_BUS
15, 16, 17, 18	GPIO	GPIO	GPIO	GPIO
30	ADC224_T0_CH0_N	ADC225_T1_CH0_N	ADC226_T2_CH0_N	ADC227_T3_CH0_N
32	ADC224_T0_CH0_P	ADC225_T1_CH0_P	ADC226_T2_CH0_P	ADC227_T3_CH0_P
35	NC	NC	NC	NC
37	NC	NC	NC	NC
42	ADC224_T0_CH2_N	ADC225_T1_CH2_N	ADC226_T2_CH2_N	ADC227_T3_CH2_N
44	ADC224_T0_CH2_P	ADC225_T1_CH2_P	ADC226_T2_CH2_P	ADC227_T3_CH2_P
47	NC	NC	NC	NC
49	NC	NC	NC	NC
23	VCM23_224	VCM23_225	VCM23_226	VCM23_227
24	VCM01_224	VCM01_225	VCM01_226	VCM01_227
others	GND	GND	GND	GND

## ZCU670

<u>Pin number</u>	<u>J17, DAC228</u>	<u>J18, DAC229</u>	<u>J19, DAC230</u>	<u>J20, DAC231</u>
3, 5	VCC12_SW	VCC12_SW	VCC12_SW	VCC12_SW
4, 6	UTIL_5V0	UTIL_5V0	UTIL_5V0	UTIL_5V0
9, 11	UTIL_3V3	UTIL_3V3	UTIL_3V3	UTIL_3V3
10, 12	VCC1V8_BUS	VCC1V8_BUS	VCC1V8_BUS	VCC1V8_BUS
15, 16, 17, 18	GPIO	GPIO	GPIO	GPIO
30	DAC227_T0_CH0_N	DAC227_T0_CH2_N	DAC228_T1_CH0_N	DAC228_T1_CH2_N
32	DAC227_T0_CH0_P	DAC227_T0_CH2_P	DAC228_T1_CH0_P	DAC228_T1_CH2_P
35	NC	NC	NC	NC
37	NC	NC	NC	NC
42	DAC227_T0_CH1_N	DAC227_T0_CH3_N	DAC228_T1_CH1_N	DAC228_T1_CH3_N
44	DAC227_T0_CH1_P	DAC227_T0_CH3_P	DAC228_T1_CH1_P	DAC228_T1_CH3_P
47	NC	NC	NC	NC
49	NC	NC	NC	NC
others	GND	GND	GND	GND

<u>Pin number</u>	<u>J21, ADC224</u>	<u>J22, ADC225</u>	<u>J23, ADC226</u>	<u>J24, ADC227</u>
3, 5	VCC12_SW	VCC12_SW	VCC12_SW	VCC12_SW
4, 6	UTIL_5V0	UTIL_5V0	UTIL_5V0	UTIL_5V0
9, 11	UTIL_3V3	UTIL_3V3	UTIL_3V3	UTIL_3V3
10, 12	VCC1V8_BUS	VCC1V8_BUS	VCC1V8_BUS	VCC1V8_BUS
15, 16, 17, 18	GPIO	GPIO	GPIO	GPIO
30	ADC224_T0_CH0_N	ADC224_T0_CH2_N	ADC225_T1_CH0_N	ADC225_T1_CH2_N
32	ADC224_T0_CH0_P	ADC224_T0_CH2_P	ADC225_T1_CH0_P	ADC225_T1_CH2_P
35	NC	NC	NC	ADC226_T2_CH01_P
37	NC	NC	NC	ADC226_T2_CH01_N
42	ADC224_T0_CH1_N	ADC224_T0_CH3_N	ADC225_T1_CH1_N	ADC225_T1_CH3_N
44	ADC224_T0_CH1_P	ADC224_T0_CH3_P	ADC225_T1_CH1_P	ADC225_T1_CH3_P
47	NC	NC	NC	ADC226_T2_CH23_P
49	NC	NC	NC	ADC226_T2_CH23_N
23	VCM23_224	VCM23_225	VCM23_226	VCM23_227
24	VCM01_224	VCM01_225	VCM01_226	VCM01_227
others	GND	GND	GND	GND

## Test points

Pfe-base features five test points for troubleshooting the power lines of the ZCU board.

<b>Ref</b>	<b>Label</b>	<b>Signal on ZCU</b>
TP1	GND	GND
TP2	12V	VCC12_SW
TP3	5V	UTIL_5V0
TP4	3V3	UTIL_3V3
TP5	1V8	VCC1V8_BUS

## Header pins

Pfe-base features two header-pin connectors J1 and J2 that provide direct access to four power lines and many digital I/O signals from the ZCU boards. Each header-pin connector has 50 positions in two rows (2x25) with 1.27 mm (0.05") pitch.

<b>Pin number</b>	<b>Header J1</b>	<b>Header J2</b>
1, 3, 5	VCC12_SW	VCC12_SW
7, 9	UTIL_5V0	UTIL_5V0
11, 13	UTIL_3V3	UTIL_3V3
15, 17	VCC1V8_BUS	VCC1V8_BUS
19	NC	ADCIO_15
21	NC	ADCIO_14
23	NC	ADCIO_13
25	NC	ADCIO_12
27	DACIO_11	ADCIO_11
29	DACIO_10	ADCIO_10
31	DACIO_09	ADCIO_09
33	DACIO_08	ADCIO_08
35	DACIO_07	ADCIO_07
37	DACIO_06	ADCIO_06
39	DACIO_05	ADCIO_05
41	DACIO_04	ADCIO_04
43	DACIO_03	ADCIO_03
45	DACIO_02	ADCIO_02
47	DACIO_01	ADCIO_01
49	DACIO_00	ADCIO_00
even pins 2–50	GND	GND

## SSMP termination

Pfe-base has two SSMP plug, male pin connectors J9 and J10. These provide a 50  $\Omega$  on-board termination rated for 50 mW (17 dBm).

## I/O expanders (GPIO)

Pfe-base hosts two I/O expanders MCP23S17 by Microchip, U1 and U2. Combined, the two I/O expanders provide 32 bidirectional general-purpose I/O (GPIO) ports. The I/O expanders are controlled through a high-speed SPI interface utilizing the signals DACIO\_12 through DACIO\_15 of the ZCU board. Refer to the datasheet for MCP23S17 (QFN package) for operation of the I/O expanders.

The controlling SPI signals from the ZCU board DACIO\_12–15 are level shifted from 1.8 V to 5 V. The resulting 32 GPIO signals are 5 V, and are routed to the eight connectors J17–J24 (4 per connector) to the PFE module boards.

<u>I/O expander pin</u>	<u>I/O expander U1</u>	<u>I/O expander U2</u>
A0, 11	GND	UTIL_5V0
A1, 12	GND	GND
A2, 13	GND	GND
*CS, 7	DACIO_15	DACIO_15
SCK, 8	DACIO_13	DACIO_13
SI, 9	DACIO_14	DACIO_14
SO, 10	DACIO_12	DACIO_12
GPA0, 17	J24 pin 17	J20 pin 17
GPA1, 18	J24 pin 15	J20 pin 15
GPA2, 19	J24 pin 16	J20 pin 16
GPA3, 20	J24 pin 18	J20 pin 18
GPA4, 21	J23 pin 17	J19 pin 17
GPA5, 22	J23 pin 15	J19 pin 15
GPA6, 23	J23 pin 16	J19 pin 16
GPA7, 24	J23 pin 18	J19 pin 18
GPB0, 25	J22 pin 17	J18 pin 17
GPB1, 26	J22 pin 15	J18 pin 15
GPB2, 27	J22 pin 16	J18 pin 16
GPB3, 28	J22 pin 18	J18 pin 18
GPB4, 1	J21 pin 17	J17 pin 17
GPB5, 2	J21 pin 15	J17 pin 15

GPB6, 3	J21 pin 16	J17 pin 16
GPB7, 4	J21 pin 18	J17 pin 18

## Power-LED

The pfe-base features an LED indicating power-on (connected to UTIL\_3V3) with mounting holes for a BIVAR SMFLP flexible light pipe assembly.

## pfe modules

### Edge-card connector

PFE modules connect to the base board pfe-base through the edge card connector J1 with the following pinout.

Pin number	Signal
3, 5	VCC12_SW
4, 6	UTIL_5V0
9, 11	UTIL_3V3
10, 12	VCC1V8_BUS
23	VCM23
24	VCM01
25, 26	NC
30	CH0_N
32	CH0_P
35	CH1_P
37	CH1_N
42	CH2_N
44	CH2_P
47	CH3_P
49	CH3_N

### SMA connectors

Edge-launch SMA connectors J2, J3, J4 and J5 expose the signals CH0, CH1, CH2 and CH3, respectively, as single-ended signals with 50  $\Omega$  impedance.

## Variants

### DAC

Module	Direction	Coupling	Range	Peak power
pfe-wide	ADC/DAC	AC	10 MHz – 10 GHz	4 dBm
pfe-wamp	DAC	AC	10 MHz – 10 GHz	16 dBm
pfe-low	DAC	DC	0 – 500 MHz	11 dBm

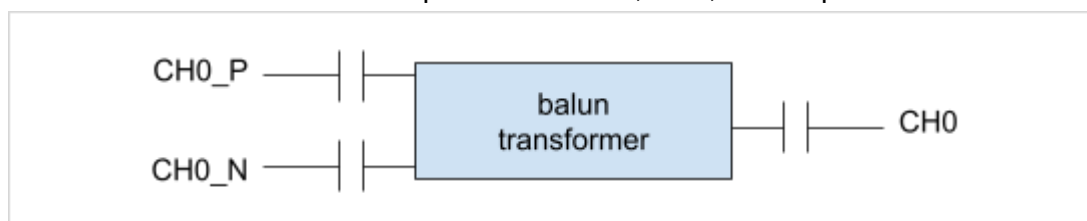
### ADC

Module	Direction	Coupling	Range	Input power for 0 dBFS*	Maximum allowed input power
pfe-wide	ADC/DAC	AC	10 MHz – 10 GHz	6 dBm	14.6 dBm
pfe-inlna	ADC	AC	10 MHz – 10 GHz	-18 dBm	-8 dBm

\* at 240MHz. Frequency dependent, see input power range curves below.

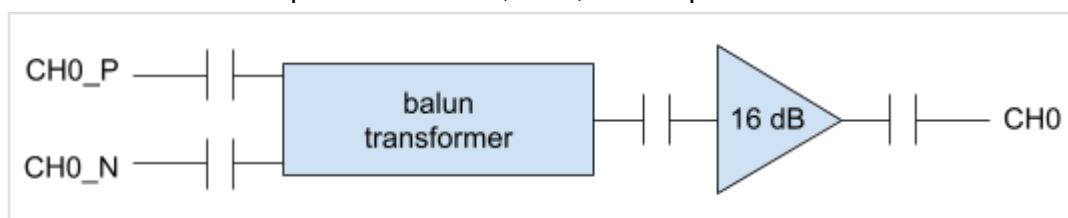
#### pfe-wide

The pfe-wide module works for both input (ADC) and output (DAC) directions. It features a wide-bandwidth balun transformer rated from 10 MHz to 10 GHz. Signals exposed through the SMA connectors are AC coupled with 100 nF, 16 V, X7R capacitors.



#### pfe-wamp

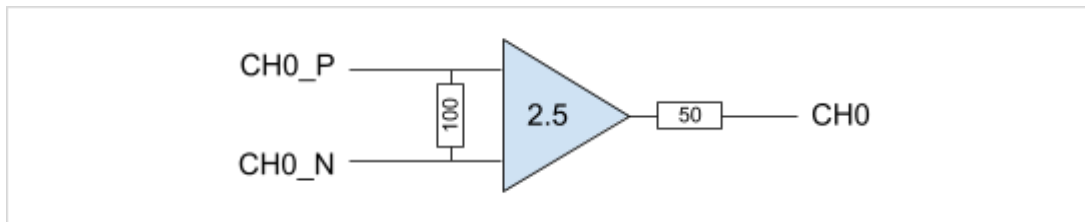
The pfe-wamp module works only for output (DAC) direction. It features the same 10MHz–10GHz balun transformer as the pfe-wide module, with the addition of the ultra-broadband amplifier GVA-123+ by Mini-Circuits. The amplifier has bandwidth 12 GHz and is suitable for low phase-noise applications. Signals exposed through the SMA connectors are AC coupled with 100 nF, 16 V, X7R capacitors.



#### pfe-low

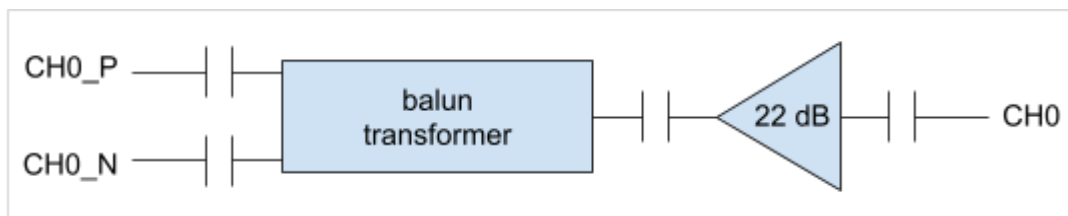
The pfe-low module works only for output (DAC) direction. It features a differential-to-single-ended amplifier with 5000 V/μs slew rate, 500 MHz full-power bandwidth and 700 MHz small-signal bandwidth. Signals exposed through the SMA connectors are DC coupled with 50 Ω source impedance. Each channel is able to drive a low-impedance load

(short) with up to 47 mA. Maximum output power is 11 dBm.



### pfe-in1na

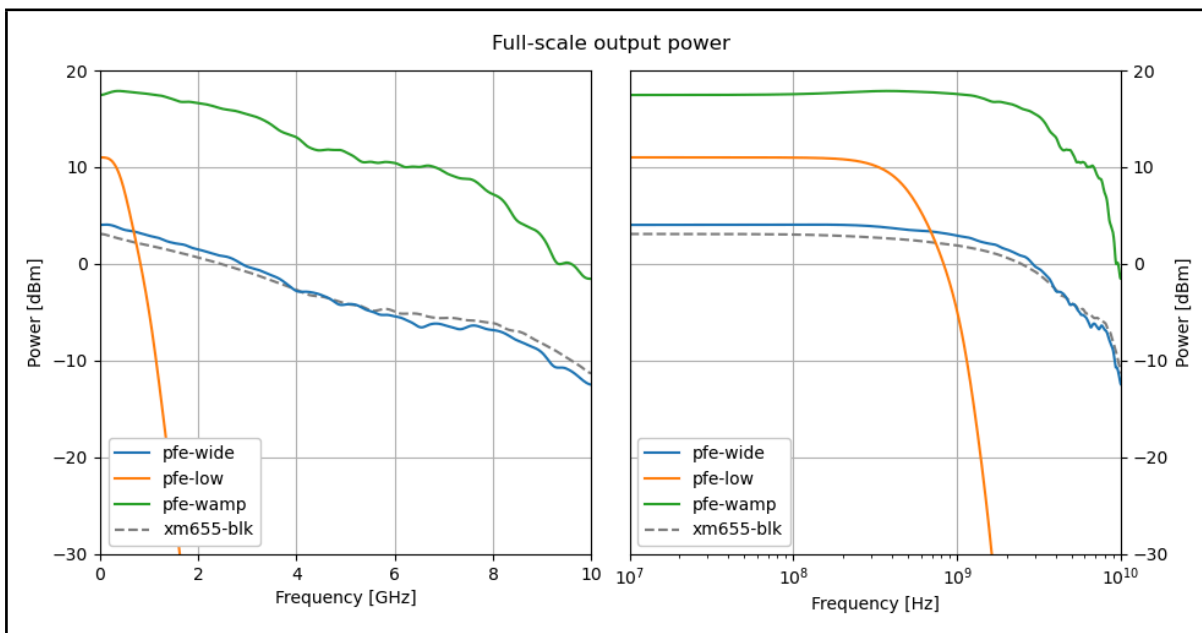
The pfe-in1na module works only for input (ADC) direction. It features the same 10MHz–10GHz balun transformer as the pfe-wide module, with the addition of the wideband, low-noise amplifier PMA3-14LN+ by Mini-Circuits. The amplifier has bandwidth 10 GHz, gain 22.6 dB and noise figure 1.8 dB. Signals exposed through the SMA connectors are AC coupled with 10 nF, 50 V, X7R capacitors. The amplifier is powered down by default. It can be powered on digitally through the GPIO expanders or by inserting jumper J6 on the module.



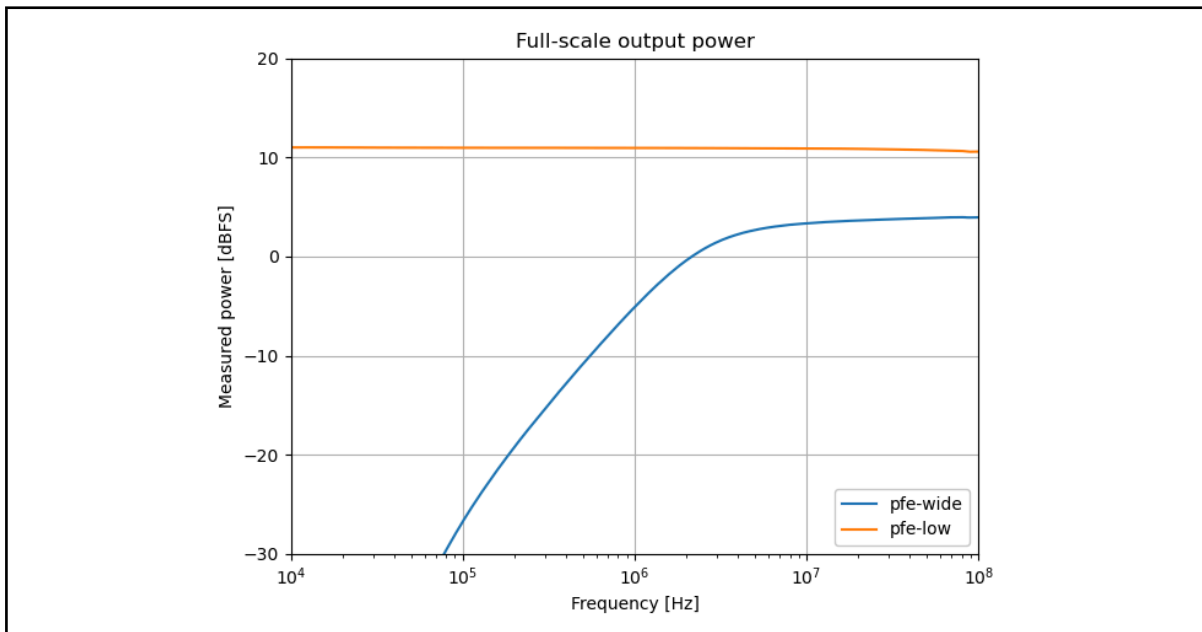
# Performance characteristics

## Output power range

Maximum output power is measured with a Rohde & Schwarz FSW spectrum analyzer, a calibrated cable, and a ZCU216 evaluation kit. Outputs are driven at full power (0 dBFS amplitude, DAC VOP set to 40 500  $\mu$ A). For comparison, output-power curves are plotted alongside measurements on the XM655 breakout board with just a DC block (no balun transformers).



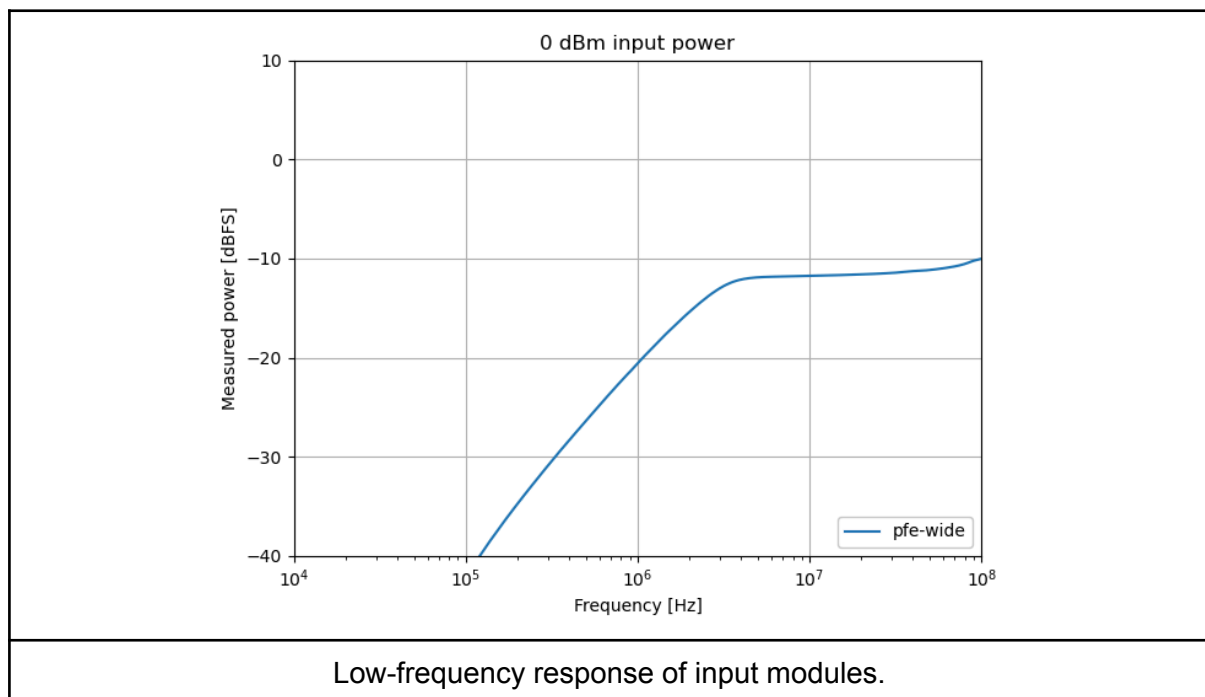
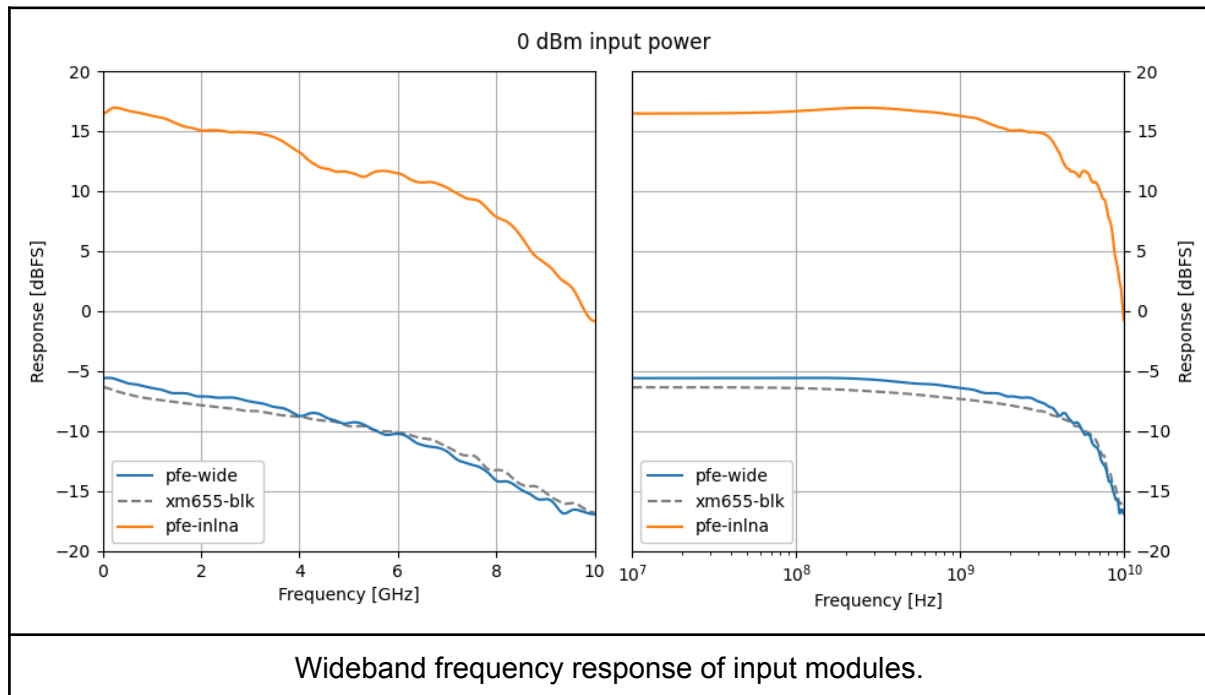
Wide-frequency response of output modules in linear (left) and logarithmic (right) scale.



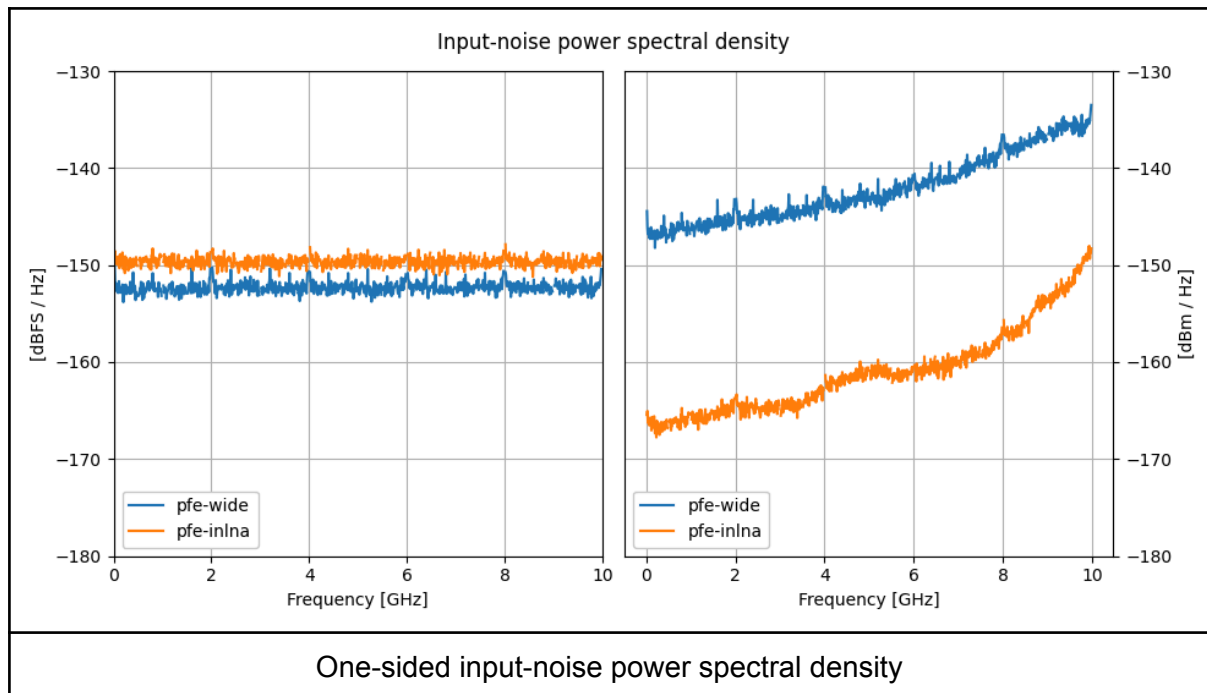
Low-frequency response of output modules.

## Input power range

Input power range is measured with a Rohde & Schwarz SGS100A signal generator, a calibrated cable, and a ZCU216 evaluation kit. Inputs have no attenuation (ADC DSA set to 0 dB). The figures show the digital response equivalent to a 0 dBm signal on the input. Actual measurements were performed at lower powers. Note that 0 dBm input power may be above maximal rating for some modules (see maximum rating above). For comparison, input-power curves are plotted alongside measurements on the XM655 breakout board with just a DC block (no balun transformers).

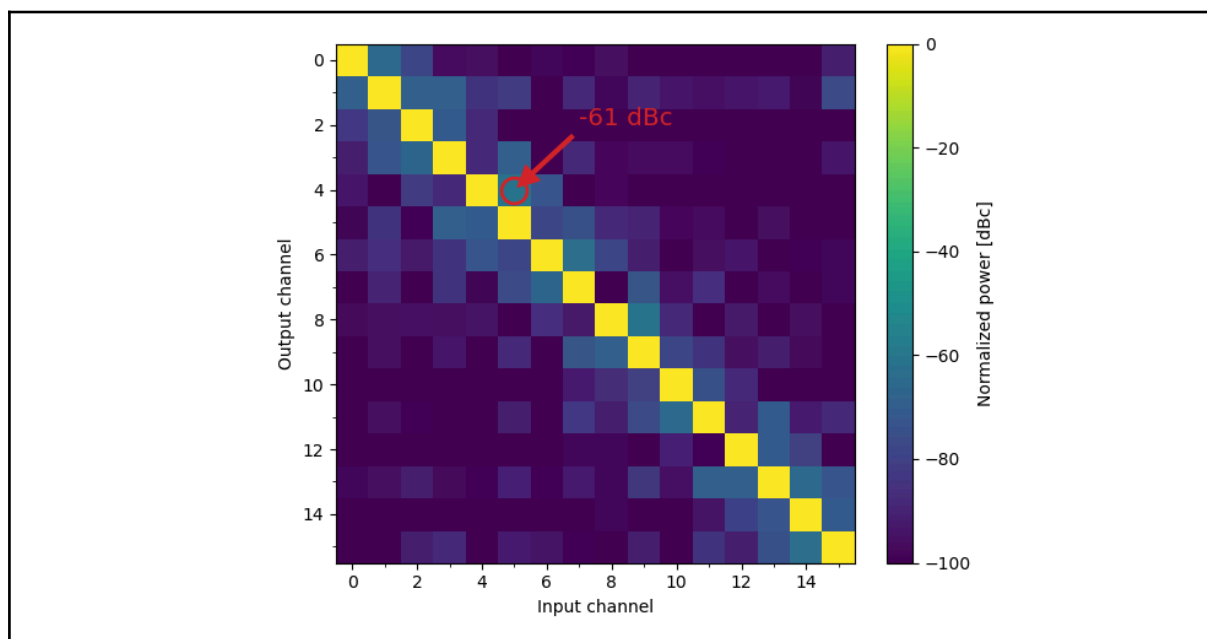


## Input noise



## Crosstalk isolation between channels

Worst-case crosstalk isolation is 61 dBc. Crosstalk is measured at 5.9 GHz in loopback configuration using a ZCU216 evaluation kit. All input and output channels use the pfe-wide module. Outputs are driven at full power (0 dBFS amplitude, DAC VOP set to 40 500  $\mu$ A), inputs have no attenuation (ADC DSA set to 0.0 dB).



Crosstalk in loopback configuration at 5.9 GHz. All input and output channels use pfe-wide modules. Worst-case across all channels -61 dBc.

## IM3: two-tone, third-order intermodulation distortion

Output tones at -6 dBFS, 20 MHz apart, DAC VOP at 20 mA, high-linearity mode. Typical.

	240 MHz	1.9 GHz	2.4 GHz	3.5 GHz	4.9 GHz	5.9 GHz
<b>pfe-wide</b>	-75 dBc	-75 dBc	-73 dBc	-71 dBc	-72 dBc	-70 dBc
<b>pfe-wamp</b>	-53 dBc	-54 dBc	-53 dBc	-54 dBc	-51 dBc	-51 dBc
<b>pfe-low</b>	-62 dBc	n/a	n/a	n/a	n/a	n/a

## Revision history

2026-04-01	Fix typos
2025-10-20	Add pfe-inlna variant. Add amplifier model name in pfe-wamp. Add information about power LED which has replaced power LED driver. Fix scaling in input range plots. Add input noise density plots. Add general handling instructions.
2023-11-15	Add IM3 data. Add information about ZCU670. Describe pinout of module connectors separately for each ZCU board. Add pfe-wamp output power range.
2023-09-27	Initial release.